WHAT IS CLAIMED IS:

1. A differential circuit including a differential amplifier circuit having a differential element provided in a signal input circuit, a constant current source connected to the differential element, and loads respectively connected to the differential element; and a source follower circuit that outputs a differential voltage based on voltage drops developing across the loads,

comprising a current supply circuit that supplies a given current to the loads connected in series with the differential element when the differential element is off.

2. A differential circuit including a first differential amplifier circuit having a first differential element provided in a signal input circuit, a first constant current source connected to the first differential element, and a first and a second loads respectively connected to the first differential element; a second differential amplifier circuit having a second differential element provided in the signal input circuit, a second constant current source connected to the second differential element, and a third and a fourth loads respectively connected to the second differential element; a first source follower circuit that outputs a first differential voltage based on voltage drops developing across the first and second loads; and a second source follower circuit that outputs a second differential voltage based on the voltage drops developing across the third and fourth loads,

comprising a first current supply circuit that supplies a given current to the first and second loads when the first differential element is off; and

a second current supply circuit that supplies the

given current to the third and fourth loads when the second differential element is off.

3. The differential circuit as claimed in claim 2, wherein each of the first and the second source follower circuits is a complementary follower circuit having two MOS transistors.

4. The differential circuit as claimed in claim 2, wherein:

the first differential element includes two N-channel MOS transistors;

the first current supply circuit is connected to gates of the two N-channel MOS transistors;

the second differential element includes two P-channel MOS transistors; and

the second current supply circuit is connected to gates of the two P-channel MOS transistors.

5. The differential circuit as claimed in claim 4, wherein equal bias potentials are applied to gate nodes of the two N-channel MOS transistors in the first current supply circuit and the gate nodes of the two P-channel MOS transistors in the second current supply circuit.

6. A receiving device having a differential circuit including a differential amplifier circuit having a differential element provided in a signal input circuit, a constant current source connected to the differential element, and loads respectively connected to the differential element; and a source follower circuit that outputs a differential voltage based on voltage drops developing across the loads,

comprising a current supply circuit that supplies a given current to the loads connected in series with the differential element when the differential element

is off.

7. A receiving device having a differential circuit including a first differential amplifier circuit having a first differential element provided in a signal input circuit, a first constant current source connected to the first differential element, and a first and a second loads respectively connected to the first differential element; a second differential amplifier circuit having a second differential element provided in the signal input circuit, a second constant current source connected to the second differential element, and a third and a fourth loads respectively connected to the second differential element; a first source follower circuit that outputs a first differential voltage based on voltage drops developing across the first and second loads; and a second source follower circuit that outputs a second differential voltage based on the voltage drops developing across the third and fourth loads,

comprising a first current supply circuit that supplies a given current to the first and second loads when the first differential element is off; and

a second current supply circuit that supplies the given current to the third and fourth loads when the second differential element is off.

8. The receiving device having the differential circuit as claimed in claim 7, wherein each of the first and the second source follower circuits is a complementary follower circuit having two MOS transistors.

9. The receiving device having the differential circuit as claimed in claim 7 or 8, wherein:

the first differential element includes two N-channel MOS transistors;

the first current supply circuit is connected to gate electrodes of the two N-channel MOS transistors;

the second differential element includes two P-channel MOS transistors; and

the second current supply circuit is connected to gates of the two P-channel MOS transistors.

10. The receiving device having the differential circuit as claimed in claim 9, wherein equal bias potentials are applied to gate nodes of the two N-channel MOS transistors in the first current supply circuit and the gate nodes of the two P-channel MOS transistors in the second current supply circuit.